2008 Solar Annual Review Meeting

Session: Wafer Silicon
Company or Organization: Georgia Tech
Funding Opportunity: University Crystalline Silicon Photovoltaics Research and Development DE-FC36-07GO17023

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Georgia Institute of Technology

Budget and Solar America Initiative Alignment

Project Beginning Date	FY07 Budget	FY08 Budget	Total Budget
October 1, 2006	$1.2 M	$900k	$2.1M

This project supports the Solar America Initiative by:

- Developing low-cost high-efficiency manufacturable cells that can attain grid parity.
- Increasing c-Si cell efficiency towards 20% to reduce the module manufacturing cost.
- Reducing the Si wafer cost and module cost by reducing the wafer thickness without compromising efficiency
- Conducting industry relevant R&D that can lead to high-efficiency production-ready large area cells.

Project Alignment with Technology Roadmap

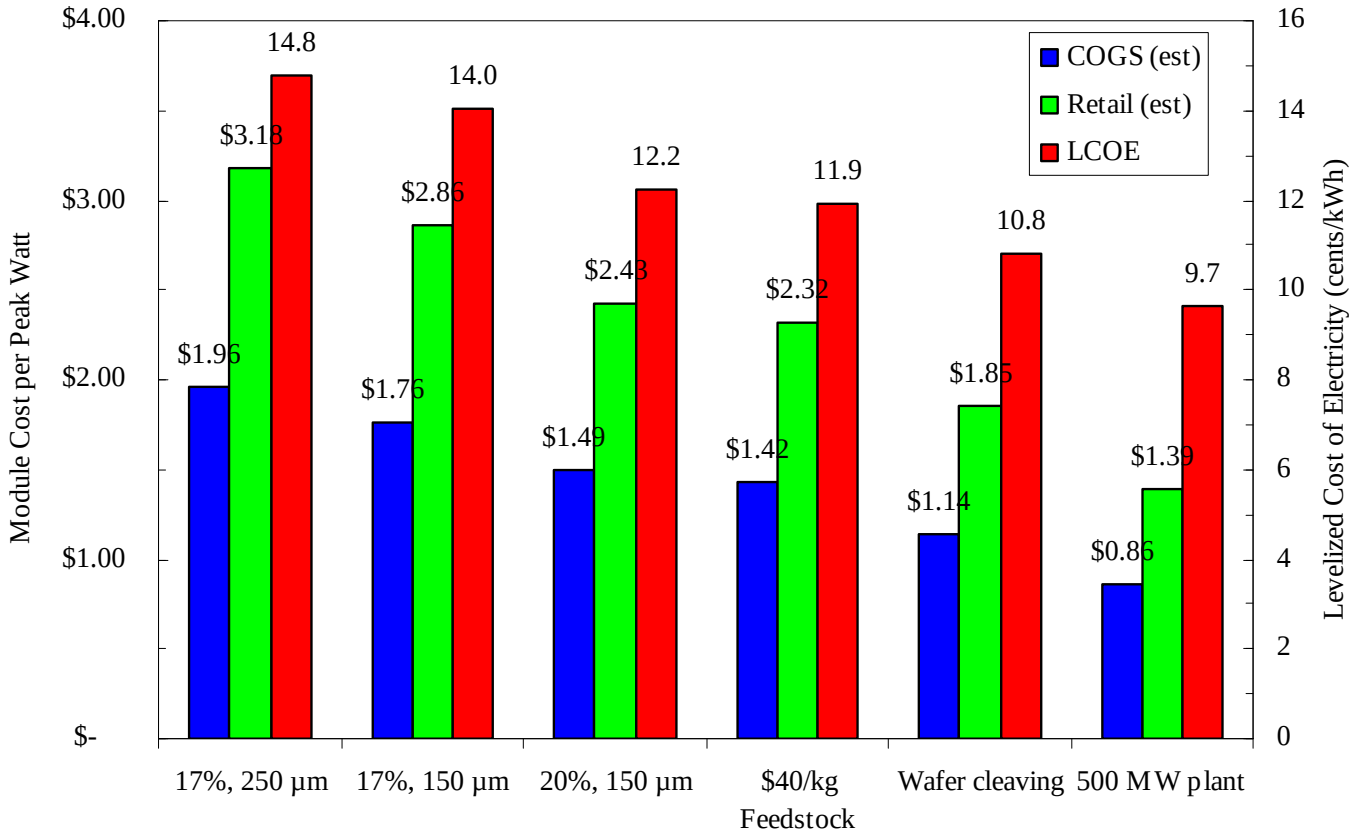
High-Efficiency Single-Crystal Cells

Wafer-Si Roadmap Need	Georgia Tech Approach
Thinner wafers and processes	Develop high-efficiency cells on thin c-Si wafers
Surface passivation & Light management for thin cells	Low-cost formation of rear contacts with a low back surface recombination velocity and a high back surface reflectance
Low recombination contacts	Develop low-cost, high-performance screen-printed metallization to high sheet resistance emitters

Low-Cost Multi-Crystalline Cells

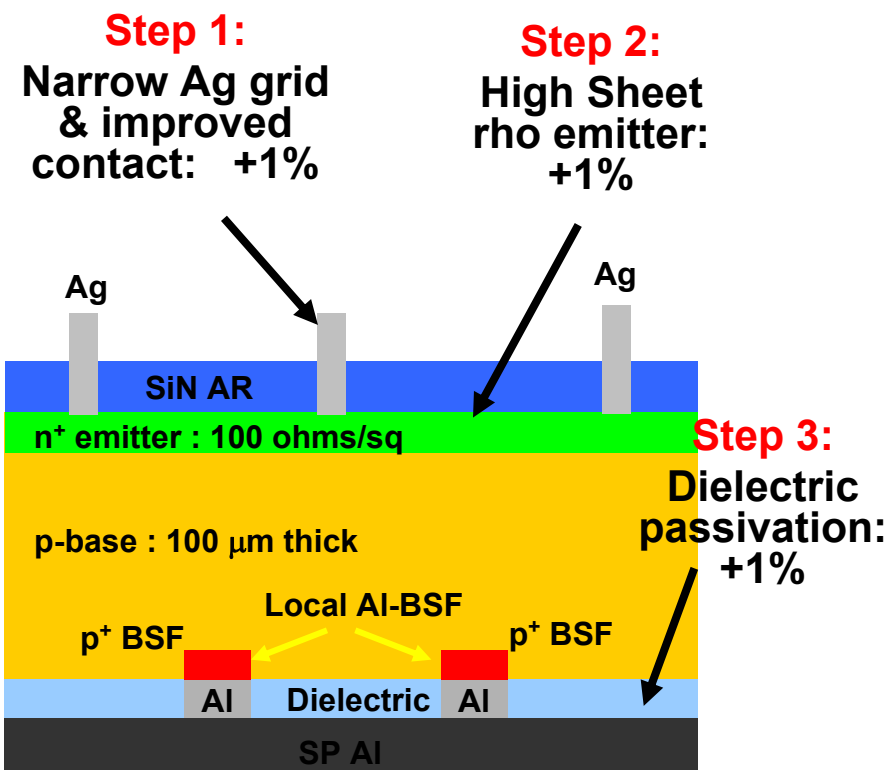
Wafer-Si Roadmap Need	Georgia Tech Approach
Bulk defect engineering	Gettering and passivation of defects in low-cost c-Si materials
Thinner wafers and processing	Develop high-efficiency cells on thin mc-Si wafers
Light management –an antireflective coating	Develop effective surface texturing and light trapping

Grid Parity with Silicon PV

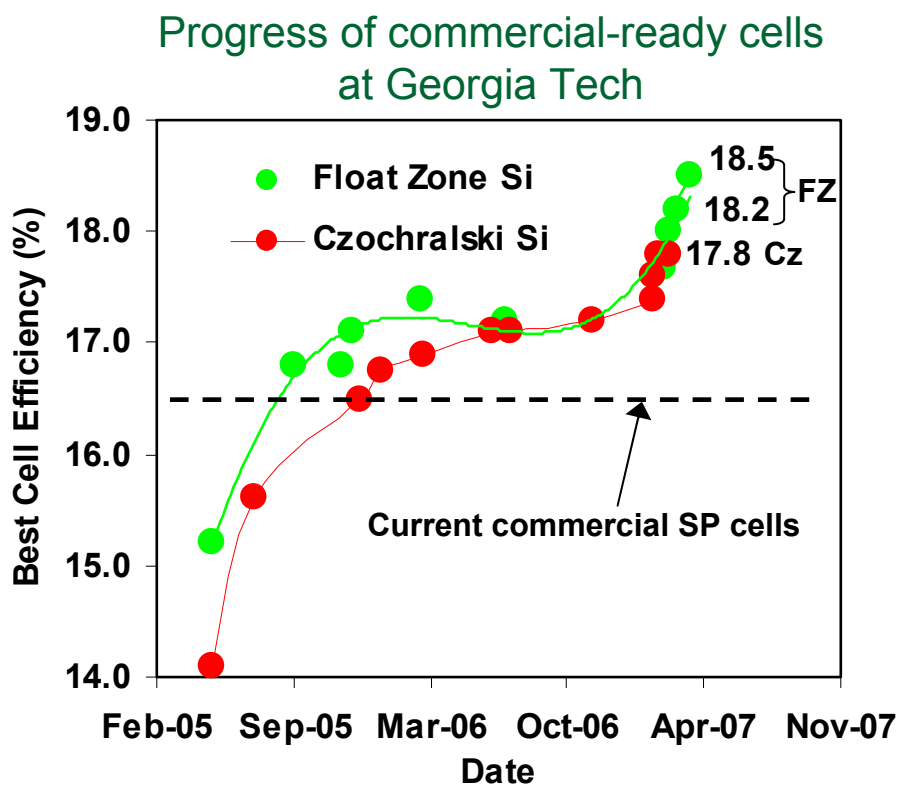


Manufacturing and retail module costs per peak watt, and estimates of the LCOE using the DOE 2015 cost estimate for BOS costs.

Project Overview: Approach to 20%-efficient Thin c-Si Cells and Progress of Commercial-ready Cells at Georgia Tech

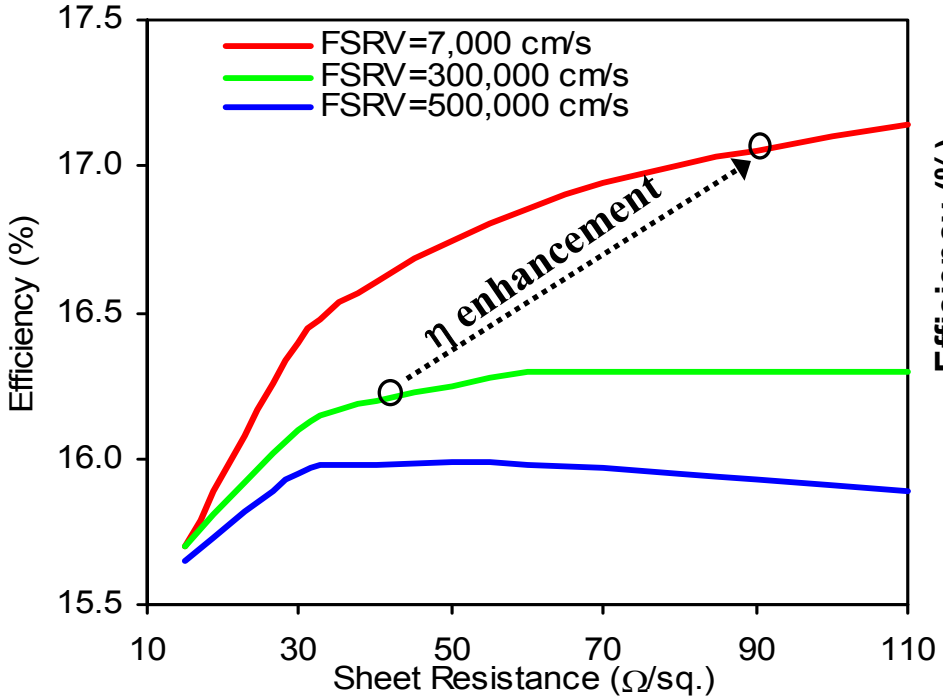


Thinning the wafer to 100 μm reduces manufacturing cost

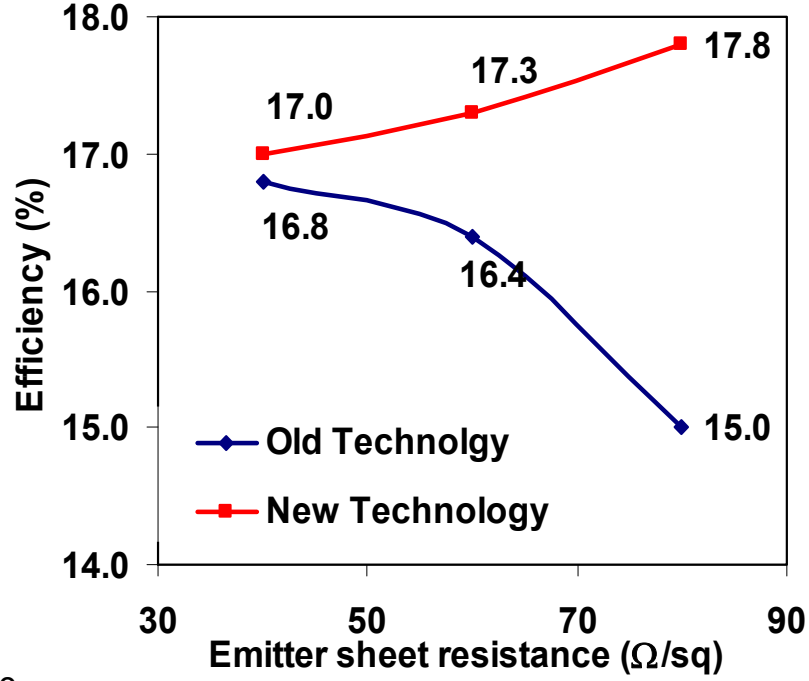


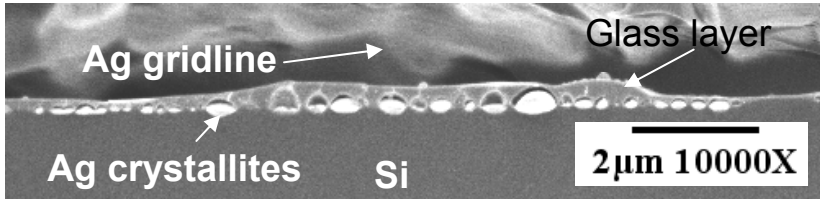
Project Overview: Screen Printed Contacts to Lightly Doped Emitters

Established Merit of High Sheet-Resistance Emitters



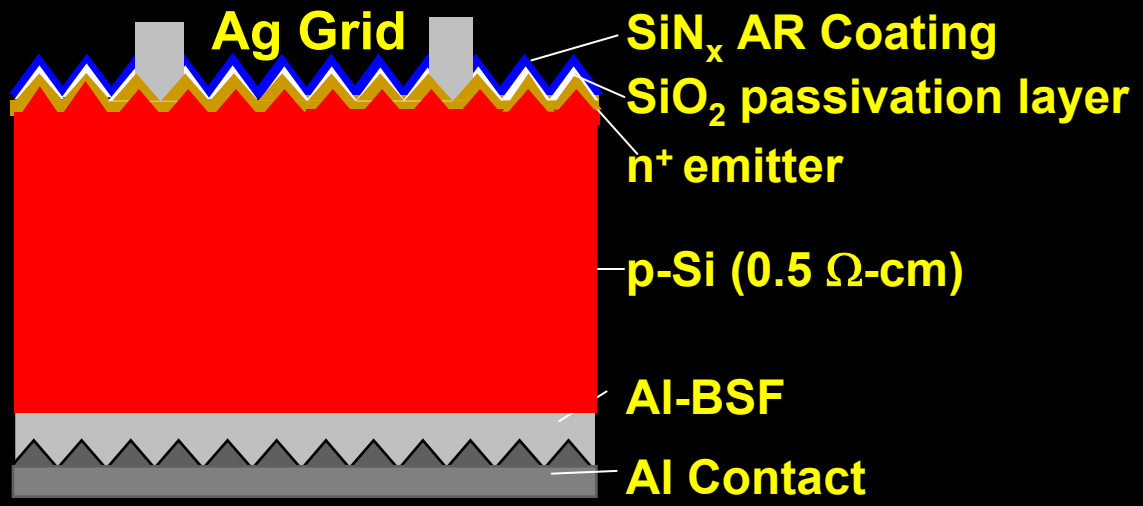
Successfully overcame high series resistance that was impairing efficiency at high sheet resistance

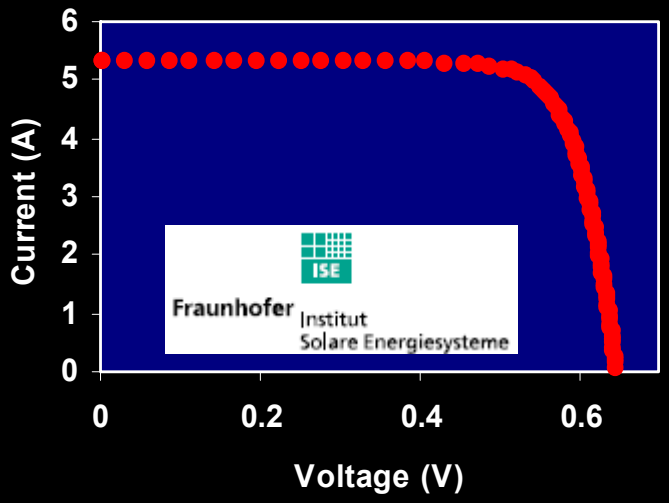




Large Area 18.2%-Efficient Cell with Screen-Printed and Co-Fired Contacts on FZ Si

Texturing
↓
$POCl_3$ Diffusion
↓
Edge Isolation
↓
Oxidation
↓
PECVD SiN_x AR
↓
Al Screen-Printing
↓
Ag Screen-Printing
↓
Belt Co-Firing





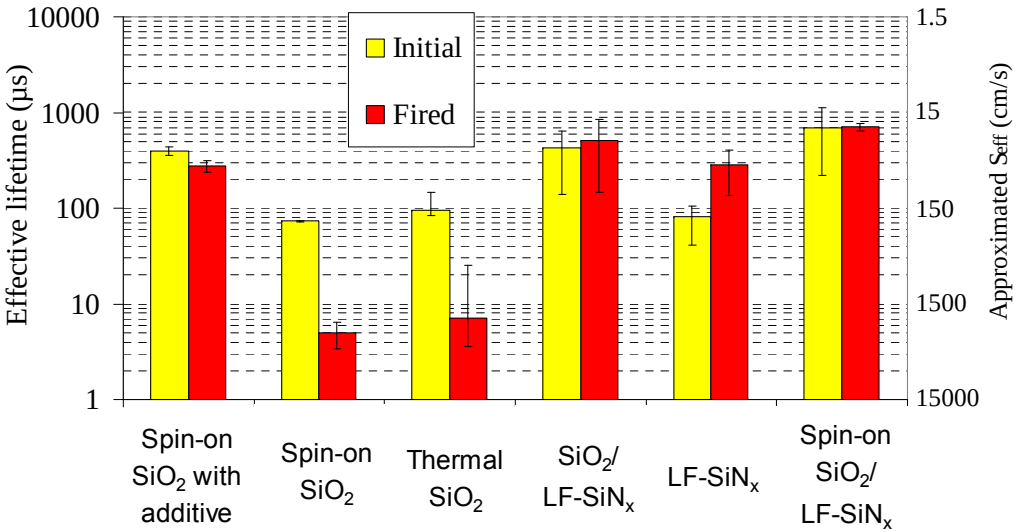
Wafer Resistivity (Ω-cm)	0.5
Cell Area (cm^2)	149
V_{OC} (mV)	648
J_{SC} (mA/cm^2)	35.8
FF	0.784
Eff. (%)	18.2

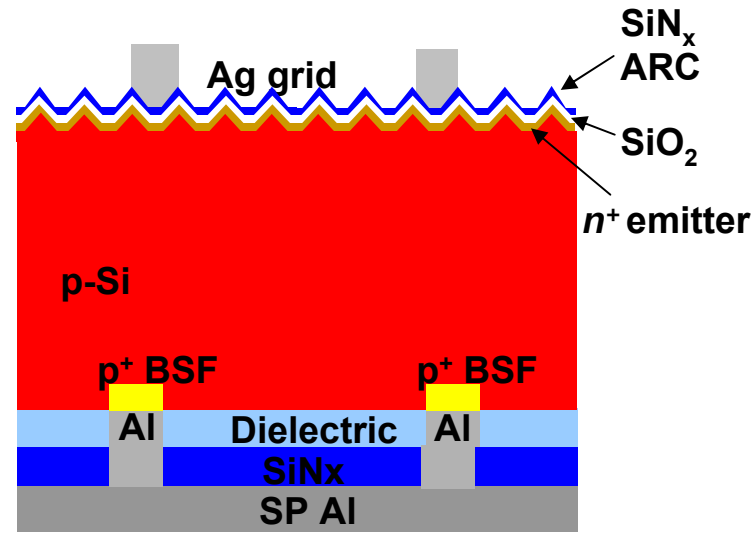
18.2% FZ cell

I-V Data

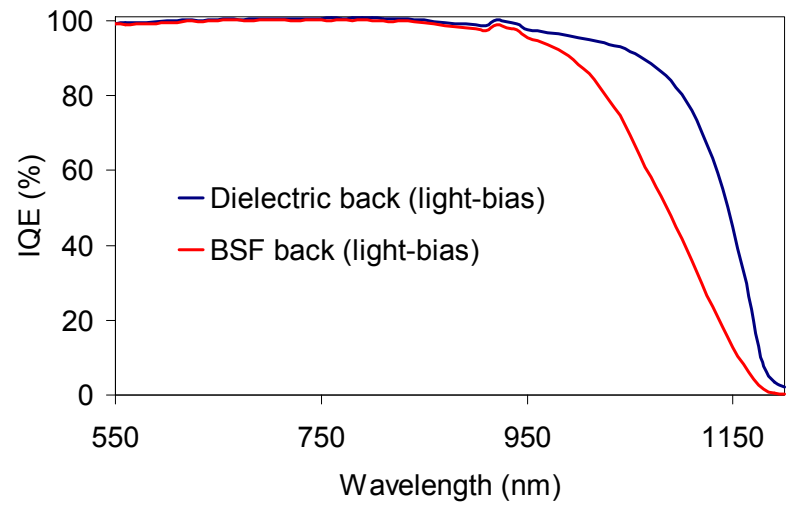
Project Overview: SiO_2-based Spin-On Dielectrics for Back Surface Passivation of p-type Si Solar Cells

SRV of dielectric stacks on Si





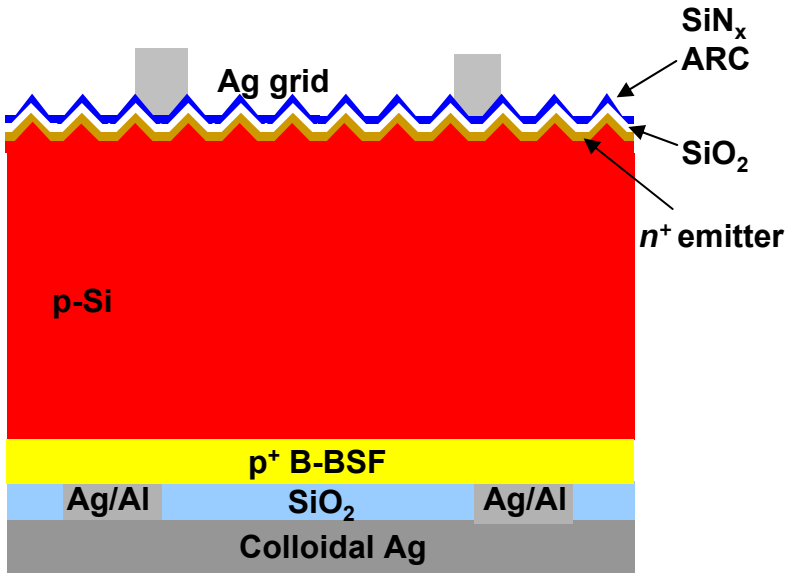
Back Contact	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
Dielectic back	653	39.1	74.5	19.0
Al-BSF	643	38.1	75.8	18.6



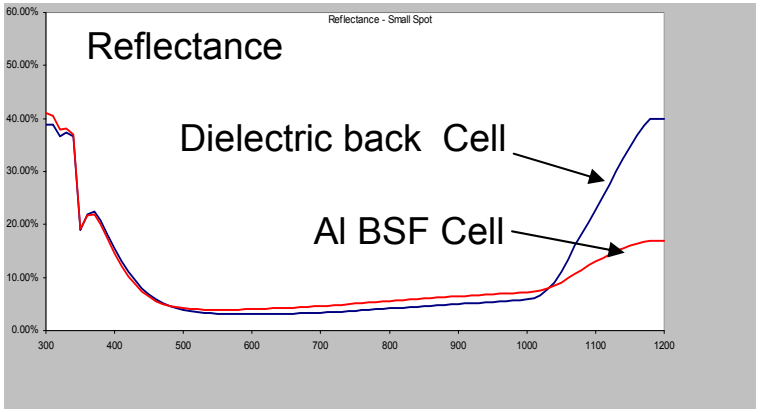
Cell Area - 4 cm^2

Reflectance

Project Overview: Light Trapping in Cells with Dielectric Passivation and Rear Local Contacts

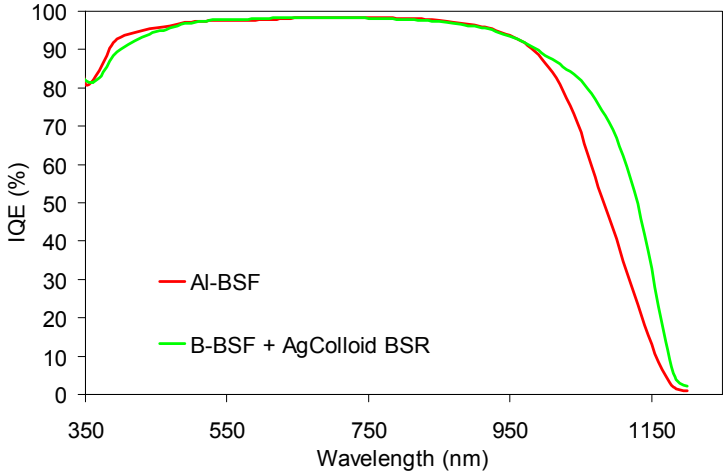


Colloidal Ag is highly scattering and results in significant light-trapping

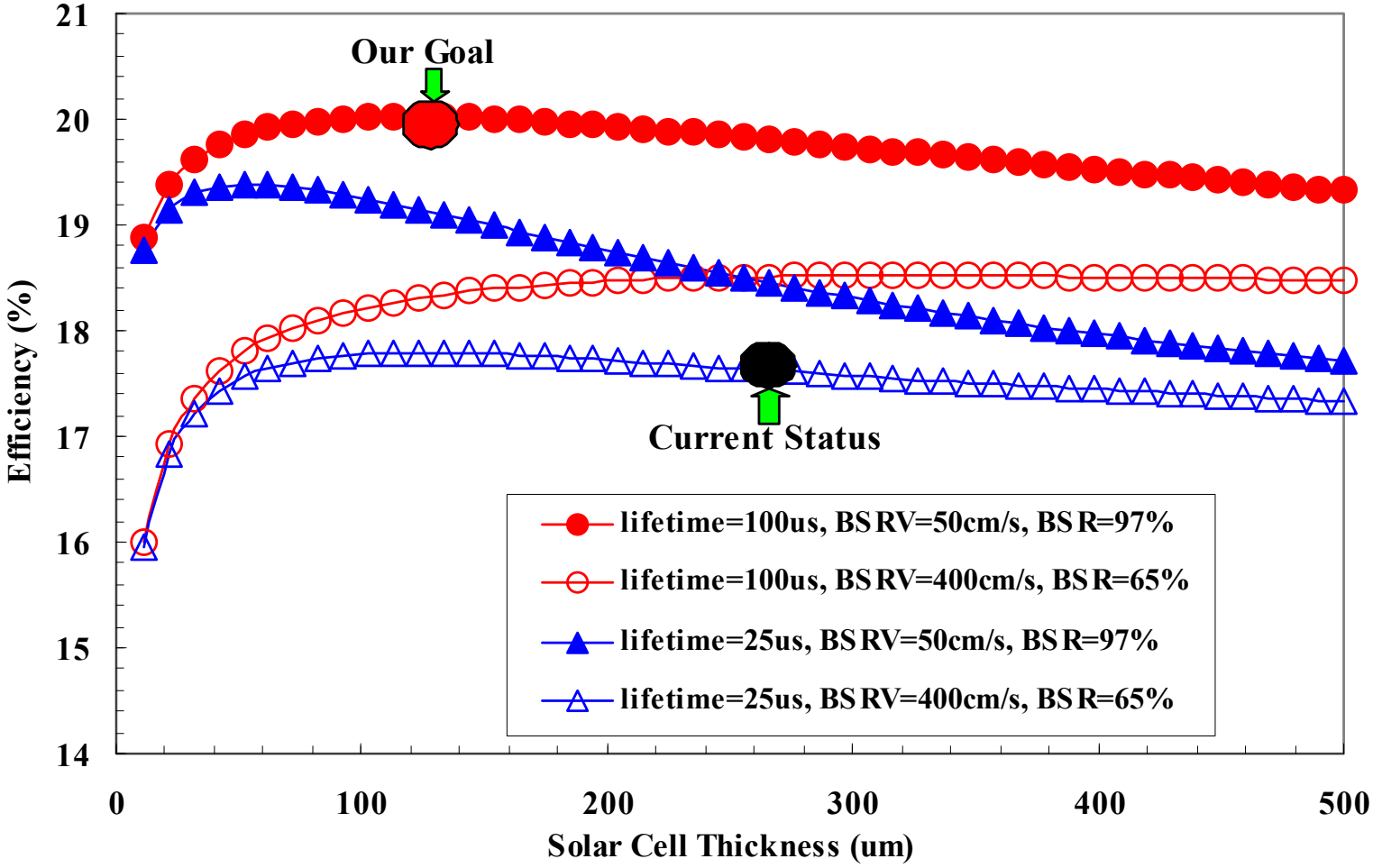


Cell Structure	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
Colloidal Ag	650	40.4	72.8	19.1
Al-BSF	639	38.1	75.8	18.5

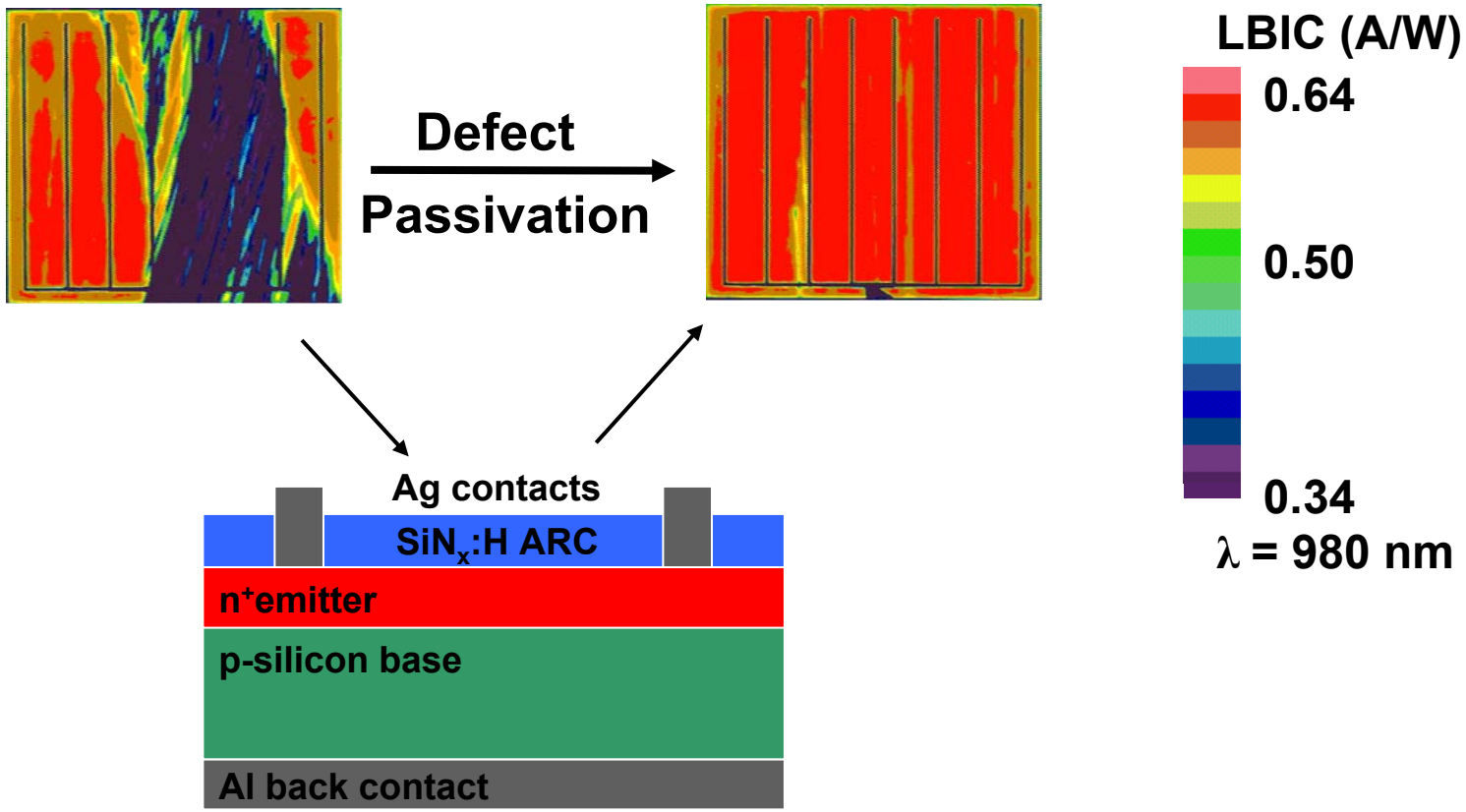
Cell Area - 4 cm^2



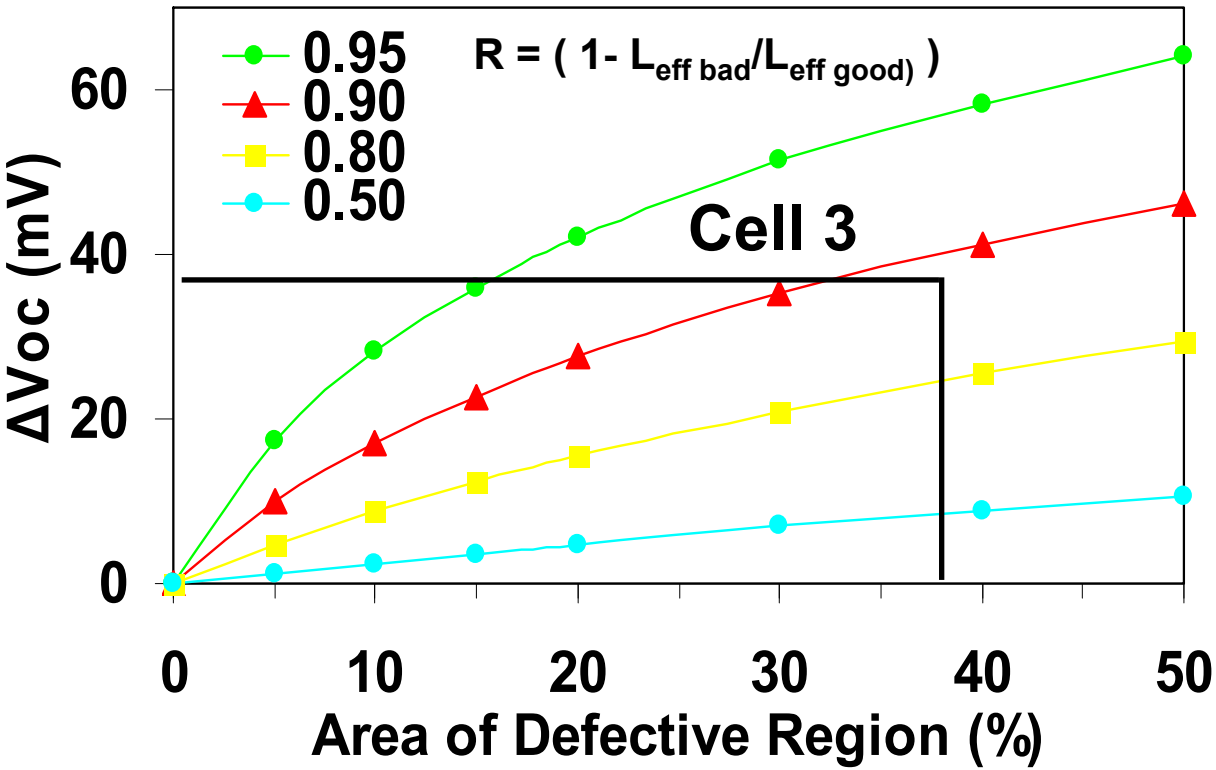
Project Overview: Bulk lifetime, thickness, BSRV and BSR targets for achieving 19-20% efficiency cells with screen printed front contacts.

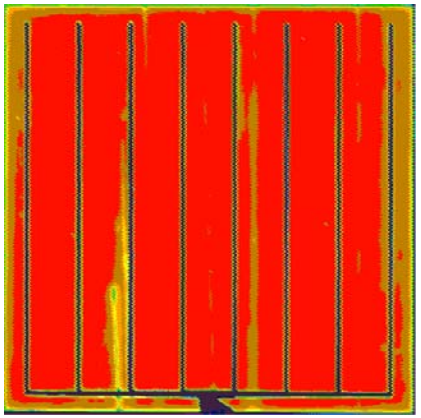


Project Overview: LBIC analysis of defects and Strategy to Fabricate high efficiency mc-Si solar cells

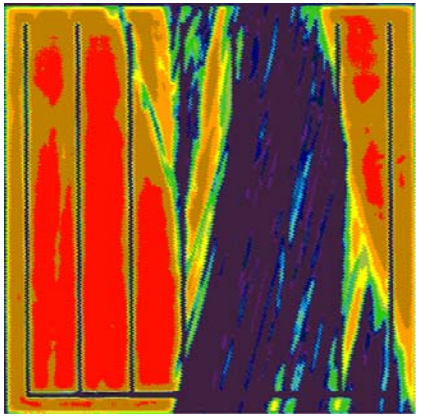


Project Overview: Loss in V_{OC} Due to Material Inhomogeneity





Cell 1



Cell 3

ID	V_{OC}(mV)	J_{SC} (mA/cm^2)	FF	Eff (%)
Cell 1	616	33.5	0.773	15.9
Cell 3	578	31.4	0.778	14.1

Project Overview: Photoluminescence scans on EFG Si Before and After RTP anneal

Process Sequence

P, SiN_x, and Al SP

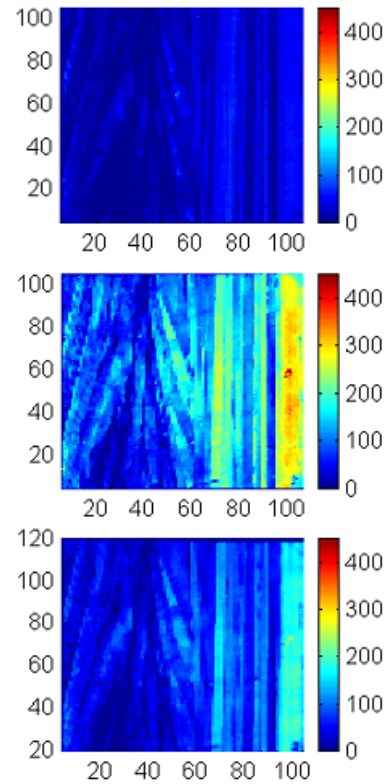
↓

RTP 750°C/1 s

↓

RTP 750°C/120 s

PL mapping



I_{bb} (avg.)

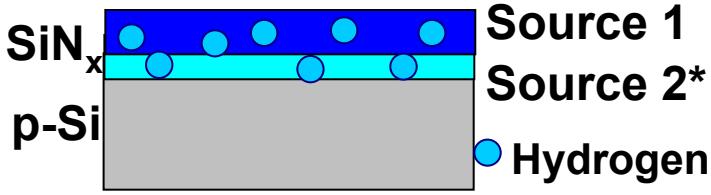
25

123

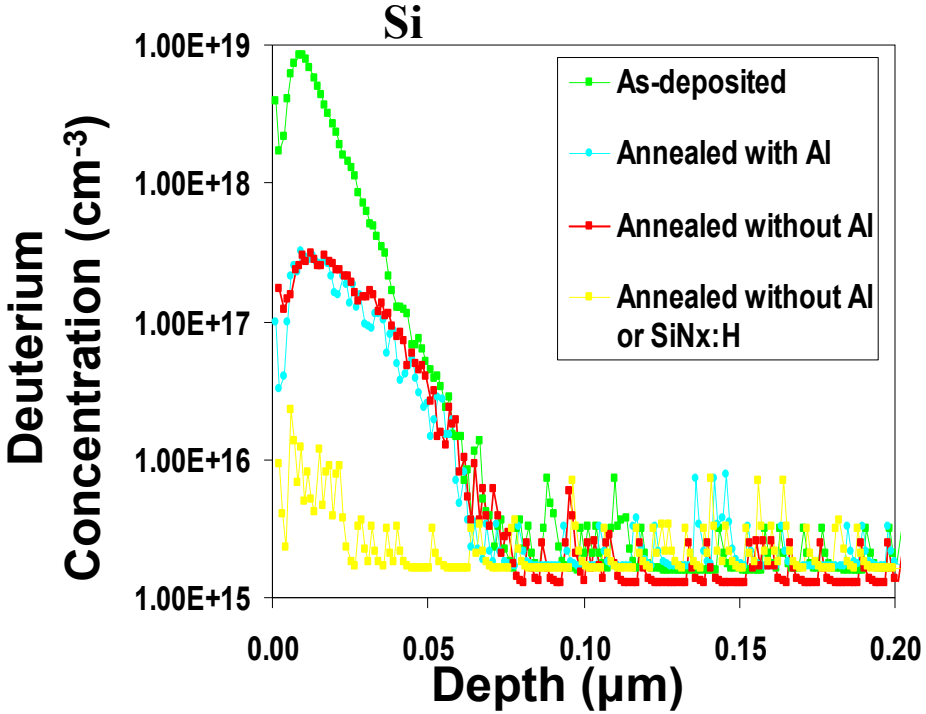
65

25 cm² EFG Si, 3.0 Ωcm, 300 µm thick

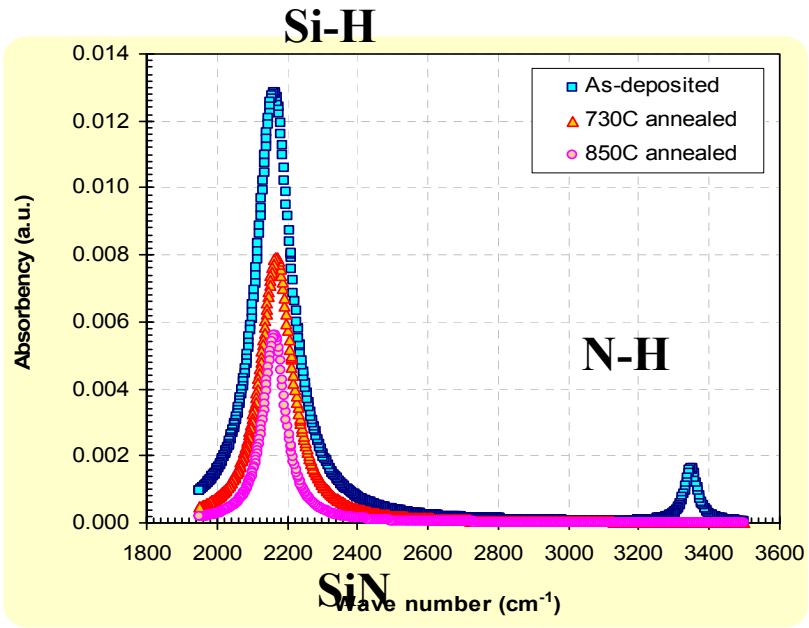
Project Overview: SIMS depth profiles of deuterium in Si and FTIR of SiN Film after deposition and anneal of LF SiN_x:H



Source 2: SIMS



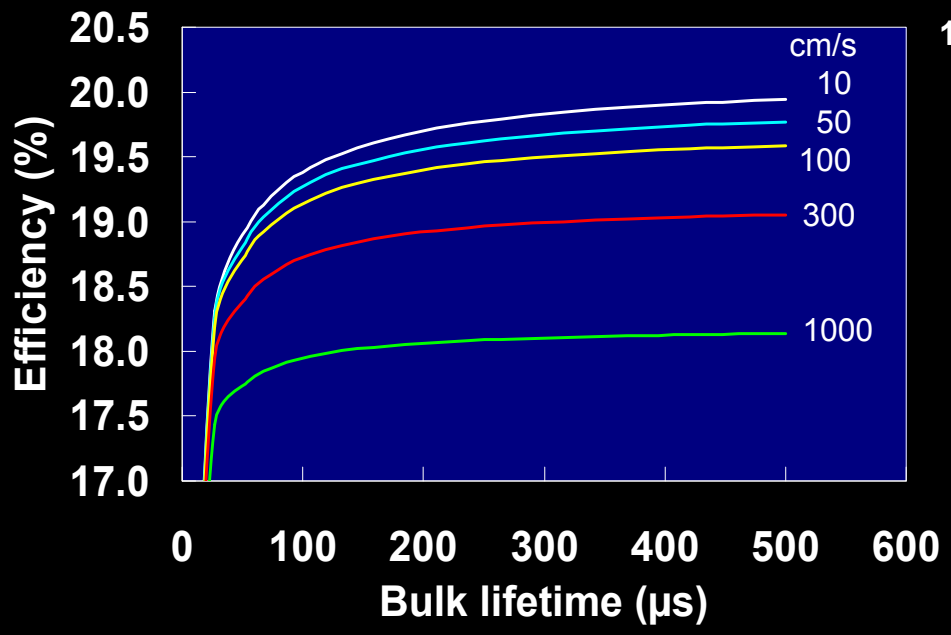
Source 1: FTIR



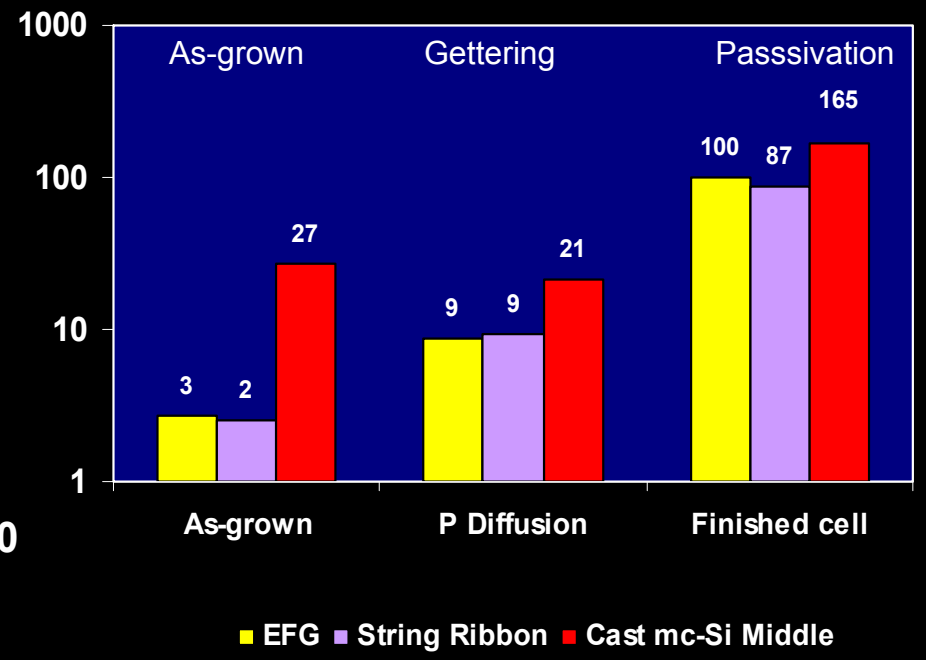
Two sources of atomic H

Lifetime requirements for high efficiency Silicon Cells

Impact of lifetime on cell efficiency



Lifetime enhancement in low-cost Si materials



Need average lifetime to >100 us. Gettering and passivation can raise lifetime from 1-5 us to >100

Project Update

	Planned work since last Program Review	Status
Past	Improve fill factor of large area cells by decreasing the contact resistance	Complete 4/30/2007
	Develope a process to achieve low surface recombination velocities on single crystal Si using any of three dielectric spin-on materials	Complete 4/30/2007
	Develop a low-cost B-BSF process that can be applied to thin cells to improve rear surface passivation	Complete 9/30/2007
	Develop a simple back surface reflector to improve light trapping in thin cells	Complete 12/31/2007
	Understand hydrogen release from PECVD SiN and diffusion through the Si wafer	Complete 1/31/2008
Future	Demonstrate a ≥0.3% absolute efficiency enhancement from texturing mc-Si	Expected 6/30/2008
	Fabricate commercial-ready cells on Cz-Si with SiO_2 passivation of the emitter with a target efficiency of 18%	Expected 6/30/2008
	Fabricate thin commercial-ready Si solar cells with efficiencies in the range of 16-17% using processes specifically design to prevent wafer breakage	Expected 6/30/2008

Obstacle Discussion

- Improve carrier lifetime stability in low-cost Cz wafers during high temperature steps.
- Develop of a surface texturing chemistry for mc-Si that reduces reflectance without increasing surface recombination.
- Improve uniformity of spin-on dielectrics on large area wafers.
- Eliminate losses associated with scale-up 19%-efficient cells from 4 cm^2 to commercial size cells ($\geq$149 cm^2).
- Reduce the number of processing steps needed to achieve 19%-efficient cells to encourage technology commercialization.
- Identify better handling tools for 125 mm thin wafers.

Major Accomplishments

- Developed a cost model to show that 18-20%-efficient thin c-Si cells can reduce the levelized cost of PV-generated electricity to 5-10 ¢/kWh.
- Developed an approach to achieve 20%-efficient cells that involves development of:
  - Narrow Ag grid & improved contacts: +1%.
  - High sheet resistance emitter: +1%.
  - Dielectric passivation and a reflective back contact: +1.
- Achieved 18%-efficient commercial-ready cells using high sheet resistance emitters.
- Developed ~19%-efficient 4 cm^2 cells with a passivated B-BSF.
- Developed 19.0%-efficient 4 cm^2 cells with rear dielectric passivation without parasitic shunting.
- Developed a clear roadmap for 20%-efficient cells.